WHAT IS CLAIMED IS:

1. An interface between an asynchronous transfer mode (ATM) network and a public switched telephone network (PSTN), comprising:

an ATM interface that communicates an ATM cell signal with the ATM network;

a vocoder that communicates a voice signal with the PSTN by a channel; and

a time division multiplex (TDM) bus that communicates a voice traffic signal between the ATM interface and the vocoder.

2. The interface of claim 1, wherein the ATM interface comprises:

a central processing unit (CPU) that disassembles the ATM cell signal or reassembles disassembled cells in real time, according to an ATM Adaptation Layer 2 (AAL2) Common Part Sublayer (CPS) protocol and a Service Specific Convergence Sublayer (SSCS) protocol, and monitors and controls other function blocks;

a memory that stores the voice traffic signal generated by a process of the CPU based on the AAL2 CPS and SSCS protocols and stores the voice traffic signal transferred from the vocoder;

a memory interface that accesses the memory for memory data input and output;

a multiplex/demultiplex unit that demultiplexes the voice traffic signal received from the memory interface and outputs a demultiplexed result to the vocoder and multiplexes the voice

traffic signal received from the vocoder and outputs a multiplexed result to the memory interface; and

a TDM interface that communicates the voice traffic signal with the vocoder over the TDM bus, synchronously with TDM timing.

3. The interface of claim 2, wherein the multiplex/demultiplex unit is further adapted to convert first parallel signals received from the memory interface into a first serial signal, convert a second serial signal received from the TDM interface into second parallel signals, and output the converted second parallel signals to the memory interface.

4. The interface of claim 2, wherein the TDM interface comprises:

an aligner that phase-aligns the voice traffic signal from the multiplex/demultiplex unit in synchronization with the TDM timing, phase-aligns the voice traffic signal from the vocoder in synchronization with the TDM timing, and outputs the phase-aligned voice traffic signal from the vocoder to the multiplex/demultiplex unit; and

a parallel/serial converter that converts first parallel voice traffic signals from the aligner into a first serial voice traffic signal, outputs the converted first serial voice traffic signal to the TDM bus, converts a second serial voice traffic signal sent over the TDM bus into second parallel voice traffic signals and outputs the second converted parallel voice traffic signals to the aligner.

5. The interface of claim 1, wherein the vocoder comprises:

a TDM interface connected to the TDM bus, the TDM interface synchronizes timings of the voice traffic signal, communicated with the ATM interface, with TDM timing and converts a serial voice traffic signal into parallel voice traffic signals;

a memory that stores the parallel voice traffic signals from the TDM interface and the voice signal from the PSTN;

a memory interface that accesses the memory to read data from or write the data to the memory; and

a CPU that periodically reads first voice data stored in the memory, transfers the read first voice data to a digital signal processor (DSP), and stores second voice data transferred from the DSP in the memory.

6. The interface of claim 2, wherein the ATM interface further comprises a most significant bit (MSB) comparator that latches a first MSB of data stored in the memory, compares the latched first MSB with a second MSB generated to read the stored data, and outputs the generated second MSB as a read MSB if the first and second MSBs are the same, thereby preventing a contention from occurring between a read operation and a write operation of the memory.

7. The interface of claim 1, further comprising a clock generator that provides a plurality of clock signals for frame synchronization and packet synchronization to the ATM interface and the vocoder.

8. A method of communicating data, comprising:

demultiplexing a multiplexed stream of first parallel data units into multiple streams of second parallel data units;

synchronizing the multiple streams of second parallel data units;

converting each of the multiple synchronized streams of second parallel data units into a stream of first serial data; and

communicating each of the streams of first serial data through a time division multiplex (TDM) bus in an assigned time slot.

9. The method of claim 8, further comprising:

generating a voice signal from each of the streams of first serial data received through the TDM bus; and

transmitting each of the generated voice signals to a destination through a public switched telephone network.

10. The method of claim 8, further comprising:

communicating each of multiple streams of second serial data through the TDM bus in an assigned time slot;

converting each of the multiple streams of second serial data units into a stream of third parallel data units; and

multiplexing the multiple streams of third parallel data units into a multiplexed stream of fourth parallel data units.

11. The method of claim 10, further comprising encoding multiple voice signals, received through a public switched telephone network, into the corresponding multiple streams of second serial data.

12. The method of claim 10, further comprising:

generating asynchronous transfer mode (ATM) packets from the multiplexed stream of fourth parallel data units; and

transmitting the generated ATM packets through an ATM network.

13. The method of claim 8, further comprising:

comparing a first address bit corresponding to data stored in a memory with a second address bit generated for the purpose of reading the stored data;

outputting the generated second address bit for use in a subsequent memory read operation if the first and second address bits have the same value, to prevent bus contention between a memory write operation and the memory read operation.

14. The method of claim 13, further comprising:

toggling the value of the second address bit if the first and second address bits have different values;

outputting the toggled second address bit for use in the subsequent memory read operation, to prevent bus contention between the memory read and write operations.

15. A communication gateway, comprising:

a multiplexer/demultiplexer (demux) that demultiplexes a multiplexed stream of first parallel data units into multiple streams of second parallel data units;

an aligner that aligns the multiple streams of second parallel data units;

a parallel-to-serial converter that converts each of the multiple aligned streams of second parallel data units into a stream of first serial data;

a time division multiplex (TDM) bus that communicates each of the streams of first serial data; and

a serial-to-parallel converter that receives each of the streams of first serial data from the TDM bus in an assigned time slot.

16. The gateway of claim 15, further comprising:

multiple vocoders that each generate a voice signal from a separate one of the streams of first serial data received by the serial-to-parallel converter; and

a public switched telephone network interface that transmits each of the generated voice signals to a destination.

17. The gateway of claim 15, wherein:

the serial-to-parallel converter communicates each of multiple streams of second serial data through the TDM bus in an assigned time slot;

the parallel-to-serial converter converts each of the multiple streams of second serial data units into a stream of third parallel data units; and

the demux multiplexes the multiple streams of third parallel data units into a multiplexed stream of fourth parallel data units.

18. The gateway of claim 17, further comprising multiple vocoders that encode multiple voice signals, received through the public switched telephone network interface, into the corresponding multiple streams of second serial data.

19. The gateway of claim 17, further comprising an asynchronous transfer mode (ATM) interface that generates ATM packets from the multiplexed stream of fourth parallel data units and transmits the generated ATM packets to an ATM network.

20. The gateway of claim 15, further comprising:

a memory that stores data; and

a comparator that compares a first address bit, corresponding to the data stored in the memory, with a second address bit generated for the purpose of reading the stored data, wherein

the comparator outputs the generated second address bit for use in a subsequent memory read operation if the first and second address bits have the same value, to prevent bus contention between a memory write operation and the memory read operation.

21. The gateway of claim 20, wherein:

the comparator toggles the value of the second address bit if the first and second address bits have different values; and

outputs the toggled second address bit for use in the subsequent memory read operation, to prevent bus contention between the memory read and write operations.